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(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; Mail Stop 68, One AMD Place, Sunnyvale, CA 94088-3453 (US).

(72) Inventor: CHEN, Maria; 3427 San Saba Drive, San Jose, CA 95148 (US).

(74) Agent: RODDY, Richard, J.; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

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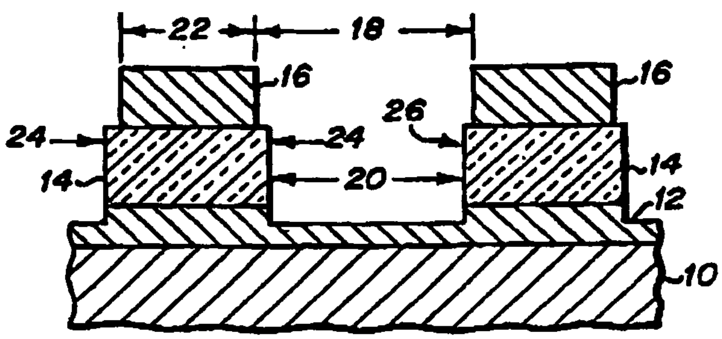
(54) Title: SILICON NITRIDE ETCH PROCESS WITH CRITICAL DIMENSION GAIN

(57) Abstract

A method for plasma etching of silicon nitride using a mixture of trifluoromethane and oxygen in a ratio of approximately 8 to 1 to selectively etch silicon nitride in preference to silicon dioxide and photoresist, resulting in critical dimension gain.



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Specification

SILICON NITRIDE ETCH PROCESS WITH CRITICAL DIMENSION GAIN

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates generally to a method for etching silicon nitride on a semiconductor wafer, and more particularly to a method for etching silicon nitride which permits critical dimension gain by preferential plasma etching of silicon nitride over silicon dioxide and photoresist with a mixture of CHF_3 and O_2.

Brief Description of the Prior Art

Semiconductor processing often involves patterning a relatively thick layer of silicon nitride coating a relatively thin layer of silicon dioxide supported upon a silicon wafer substrate. The nitride layer is covered with a photoresistant material, and this masking layer is patterned with apertures in accordance with the desired silicon nitride pattern. Such a process is described in U.S. Patent Number 4,484,979 (Stocker), which discloses a two-step method for patterning silicon nitride in a multifaceted etching chamber without penetrating through the underlying silicon dioxide layer. In the first step, relatively fast etching is accomplished through reactive

ion etching (RIE) using trifluoromethane (CHF_3) and oxygen (O_2) in ratios of 1:1 to 5.7:1. In a second etching step, silicon nitride is more selectively etched with respect to silicon dioxide and photoresist, using a mixture of oxygen to CHF_3 which is at least 9:1. *Stocker* accomplishes high selectivity of nitride to oxide etching in this second etch step, and thereby minimizes widening of apertures in the nitride layer (*i.e.* minimizes loss of linewidth control).

Barber et al., U.S. Patent Number 4,966,870, describe selective reactive ion etching of silicon nitride over borophosphosilicate glass and titanium disilicide using a CHF_3/O_2 mixture. *Baldi et al.*, U.S. Patent Number 4,897,365, teach a method for reducing bird beaks (oxide wedges) formed during a planox process using selective etching of silicon nitride over silicon oxide with reactive ion etching using a CHF_3/CO_2 mixture. Silicon nitride patterning with photoresist and reactive ion etching of silicon nitride is well known to those skilled in the art, and the disclosures of *Stocker*, *Barber et al.* and *Baldi et al.* describe the such processes in substantial detail.

SUMMARY OF THE INVENTION

It is the primary object of the present invention to provide an improved method for removal of silicon nitride from a semiconductor substrate.

Another object to the present invention is to provide an improved method for removal of silicon nitride in preference to photoresist and silicon oxide in the processing of a semiconductor substrate.

A further object to the present invention is to provide a silicon nitride etch process which results in critical dimension gain.

Briefly, the preferred embodiment of the present invention is a method for plasma etching of silicon nitride using a mixture of trifluoromethane and oxygen in a ratio of approximately 8 to 1 to selectively etch silicon nitride in preference to silicon dioxide and photoresist.

IN THE DRAWING

FIG. 1 illustrates a semiconductor substrate patterned with photoresist prior to etching of silicon nitride;

FIG. 2 illustrates a semiconductor substrate after etching in accordance with the process of the present invention;

FIG. 3 shows the etch rates for silicon nitride, silicon dioxide, and photoresist using the process of the present invention;

FIG. 4 is a graph showing etch uniformity and selectivity using the process of the present invention; and

FIG. 5 shows the critical dimension gain obtained with the process of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

This invention provides a method for removal of silicon nitride through plasma etching with a mixture of CHF_3 and O_2. The method selectively removes silicon nitride in preference to photoresist and silicon dioxide and provides critical dimension gain.

With reference to FIG. 1, a silicon semiconductor substrate patterned with photoresist is shown. Silicon substrate 10 supports a layer of silicon dioxide 12 which is approximately 150 to 250 Angstroms thick. A silicon nitride layer 14 of approximately 1800 to 2000 Angstroms is situated on top of the silicon dioxide layer 12. On top of the silicon nitride layer 14 is a layer of photoresist 16 having a thickness of 0.7 to 1.2 micrometers (700 nanometers to 1200 nanometers). The layers are not drawn to scale in order to show the features of the invention more clearly. The measurements discussed below involve KTI I-line positive photoresist, but the critical dimension gain is found with other resists as well.

The photoresist layer 16 has been patterned to leave apertures that are not covered by photoresist and other areas covered by photoresist. A typical aperture as

indicated by 18 is on the order of 0.8 to 1.0 micrometers. The width of the photoresist line indicated by 22 is typically on the order of 0.5 micrometers. As noted above, it is particularly desirable to minimize widening of apertures in the nitride layer 18 and thereby minimize loss of control of the linewidth 22. The width 22 is known as the developed inspection critical dimension (DICD), indicating that it is the width of the line 22 after photo mask development (i.e. after photoresist patterning). In the preferred embodiment of the present invention, after photoresist patterning the silicon nitride layer 14 and photoresist layer 16 are subjected to plasma etching in a single-step nitride etch process using a CHF_3 flow of 80 sccm (standard cubic centimeters per minute) and an O_2 flow of 10 sccm. The gas pressure is approximately 40 millitorr and the discharge is 700 watts with a magnetic field of 20 Gauss. The etching is preferably conducted in a single wafer plasma etcher, where uniformity of etch conditions is easier to achieve than in a multifaceted etching chamber for etching multiple wafers.

Referring now to FIG. 2, the structure on the silicon substrate 10 is shown after plasma etching in accordance with the method of the present invention.. Silicon nitride has been removed in the areas where it is not masked by photoresist 16. There has been some etching through the

nitride, leaving some silicon dioxide (50 to 170 Angstroms). FIG. 2 illustrates that the width of the photoresist 22 is slightly less than the width of the remaining silicon nitride 14. In particular, the method of the present invention will result in a critical dimension of the silicon nitride 24 which is wider than the critical dimension 22 of the photoresist. In a photoresist line of approximately 0.50 micrometers (500 nanometers), the width of the underlying silicon nitride will be approximately 0.55 micrometers (550 nanometers), a critical dimension gain of 50 nanometers. Although the preuse mechanism is not known, the chemistry and operating regime cause the critical dimension gain.

When the photoresist 18 is removed in the next process step, the present invention results in final inspection critical dimension (FICD) gain ranges from 30 to 80 nanometers over the developed inspection critical dimension (DICD). This is in contrast to prior art etch processes which usually experience at least some critical dimension loss. When there is a critical dimension loss from the drawn line on a photoresist mask to the finished product, a greater area of the silicon wafer is necessary to create a particular device. Therefore, the critical dimension gain achieved with the present invention permits higher resolution and smaller device size.

We have found that plasma etching using a mixture of CHF_3 to O_2 in the ratio of at least 6:1 up to 15:1 will provide a satisfactory result with regard to silicon nitride removal and critical dimension gain. Ratios in the range of 6:1 to 10:1 are preferred. The pressure is preferably less than 100 mTorr, and most preferably in the range of 20 to 60 mTorr. The RF power density range is preferably 0.6 to 1.1 W/cm^2. The optimal process conditions are shown in Table 1:

Table 1:

CHF_3 (SCCM)	80
O_2 (SCCM)	10
Power (Watt)	700
Pressure (mTorr)	40
Magnetic Field (Gauss)	20
Endpoint/Time (sec)	27*

*depends on the actual endpoint, this is only an average number for 1350 Å nitride thickness.

The results of the use of this process are a nitride etch rate of approximately 2950 Angstroms per minute, good uniformity of nitride, an oxide etch rate of approximately 1500 Angstroms per minute (selectivity of nitride to oxide is 2:1). The resist etch rate is approximately 1230 Angstroms per minute when measured on oxide. Therefore, the actual etch rate

for resist on nitride is much lower (on the order of 500 Angstroms/minute), and the total resist loss is not a concern during the relatively short etching time (approximately 30 seconds). The final inspection critical dimension gain is on the order of 0.06 to 0.16 micrometers from the developed inspection critical dimension. The variation from dense area to large isolated area on the substrate is minimal, with an etch profile of 89° to 90° in the dense area and 82° to 86° in the large isolated area (the angle is that of nitride profile 26 (after photoresist stripping) to the horizontal).

Notably, the present invention is a one step process that considerably simplifies the nitride etch over two step processes. A one step process provides much easier handling. Since the time for the etch is relatively short (around 30 seconds), even though the etch rate is lower in a one step process than in the fast etch step of a two step process, there is not much sacrifice in throughput because there is no need to change reactants/conditions with a one step process.

FIG. 3 illustrates the results obtained with the single etch process in a number of different tests. The graph shows silicon nitride, silicon oxide and resist etch rates. FIG. 4 shows etch uniformity and selectivity of nitride/oxide and nitride/photoresist. The nitride etch uniformity is shown in percent and refers to variations across the processed wafer substrate.

FIG. 5 shows the critical dimension gain with the process of the present invention with 0.7 to 0.8 micron linewidths and 1.4 to 1.6 micron linewidth. As noted above, the method shows critical dimension gain in the final inspection over the developed inspection critical dimension.

Although the present invention has been described above in terms of a specific embodiment, it is anticipated that alterations and modifications thereof will no doubt become apparent to those skilled in the art. It is therefore intended that the following claims be interpreted as covering all such alterations and modifications as fall within the true spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A method for etching a silicon nitride layer on a silicon substrate, comprising the steps of:

(a) growing a layer of oxide on the substrate;

(b) depositing a layer of silicon nitride on the oxide layer;

(c) creating a patterned photoresist layer on the silicon nitride layer;

(d) plasma etching the patterned photoresist and silicon nitride layers with a gas mixture comprising trifluoromethane and oxygen in a ratio of at least 6:1, thereby selectively removing the silicon nitride which is not covered by photoresist.

2. The method of claim 1, further comprising the step of removing the photoresist after the etching step is completed.

3. The method of claim 2, further comprising the step of growing a field oxide layer over areas of exposed oxide after the photoresist removal step is completed.

4. The method of claim 1, wherein the pressure at which the etching step is performed is less than 100 millitorr.

5. The method of claim 1, wherein the power density in the etching step is in the range of 0.6 to 1.1 W/cm^2.

6. The method of claim 1, wherein the ratio of trifluoromethane to oxygen is in the range of 6:1 to 10:1.

7. The method of claim 6, wherein the pressure at which the etching step is performed is less than 100 millitorr.

8. The method of claim 6, wherein the power density in the etching step is in the range of 0.6 to 1.1 W/cm^2.

9. The method of claim 6, further comprising the step of removing the photoresist after the etching step is completed.

10. The method of claim 9, further comprising the step of growing a field oxide layer over areas of exposed oxide after the photoresist removal step is completed.

11. The method of claim 10, wherein the pressure at which the etching step is preformed is less than 100 millitorr.

12. The method of claim 11, wherein the power density in the etching step is in the range of 0.6 to 1.1 W/cm^2.

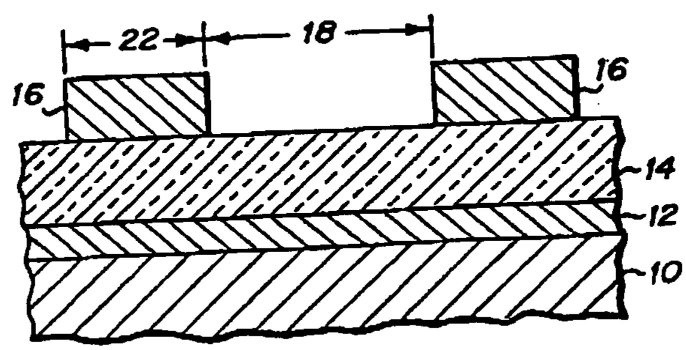

Fig_1

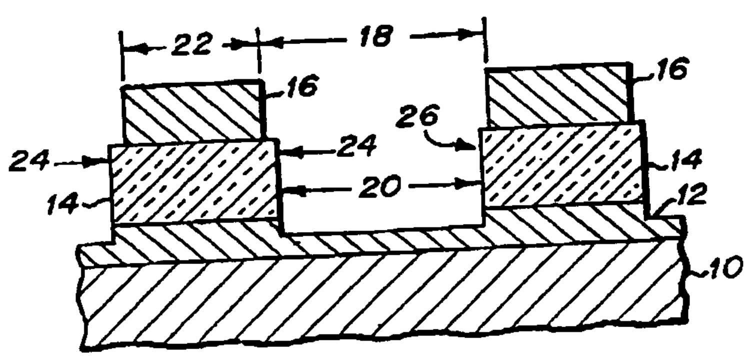

Fig_2

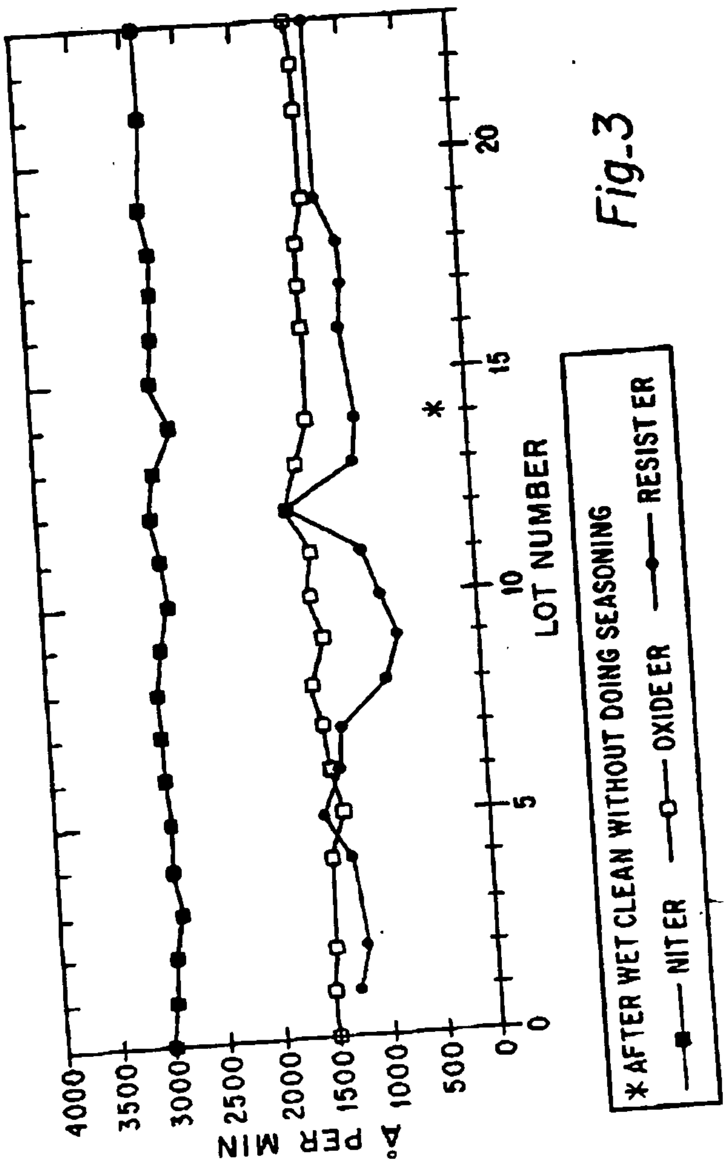
Å PER MIN
4000
3500
3000
2500
2000
1500
1000
500
0
0
5
10
15
20
LOT NUMBER
*
* AFTER WET CLEAN WITHOUT DOING SEASONING
NIT ER
OXIDE ER
RESIST ER

Fig. 3

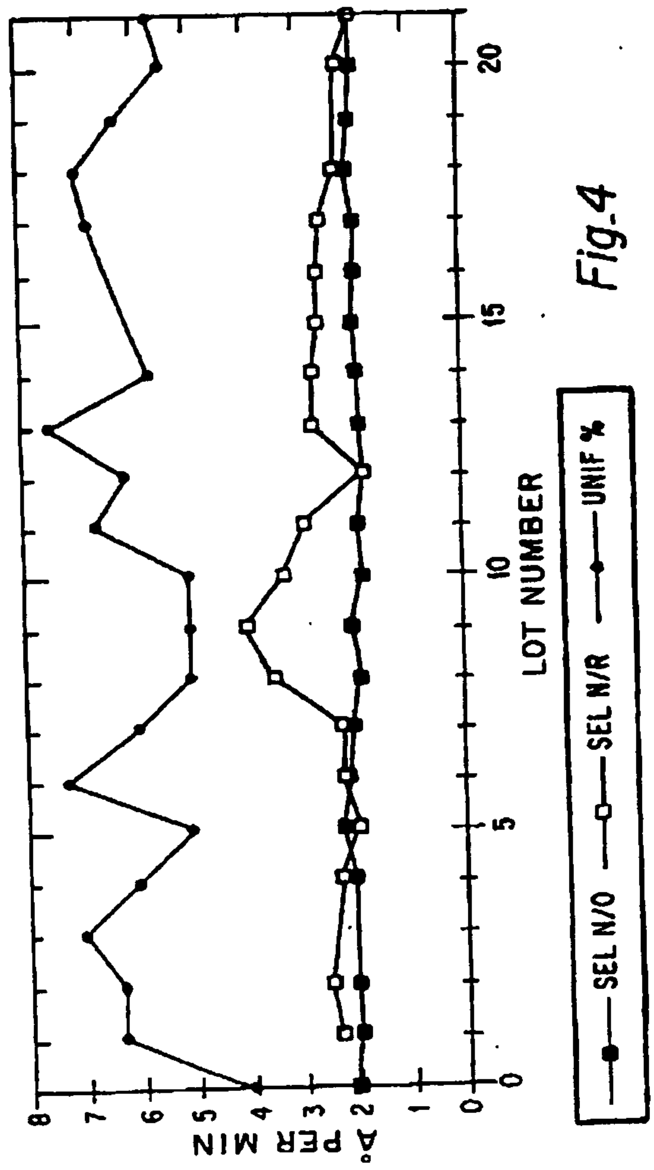

Fig.4

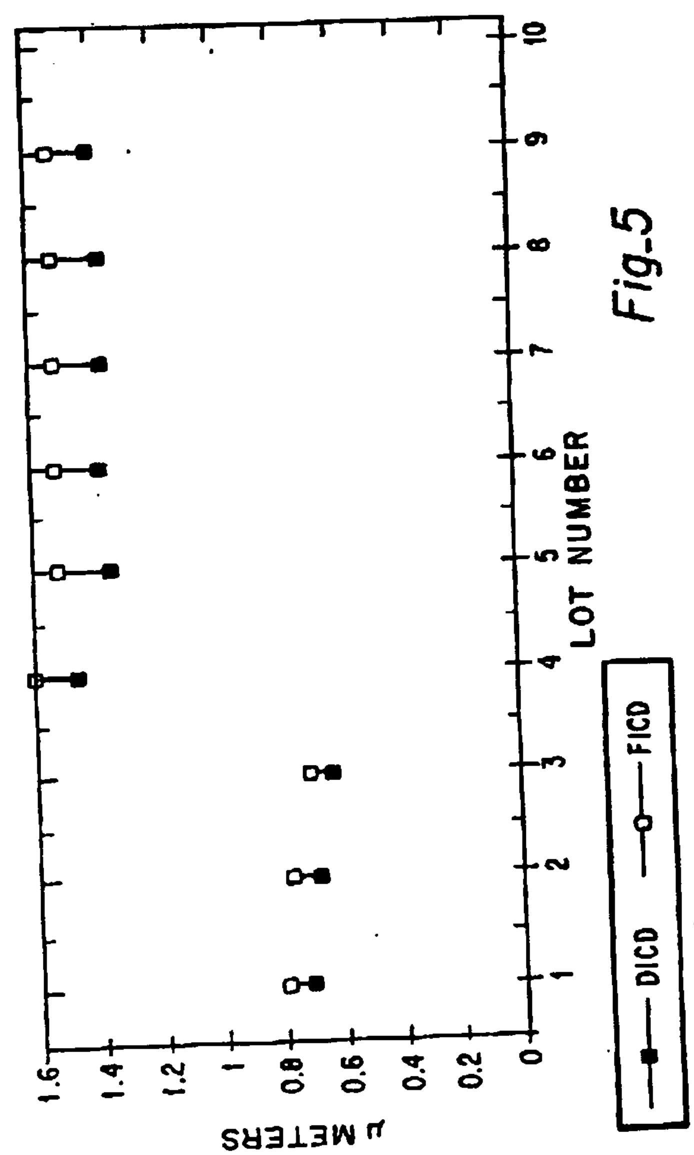

Fig_5

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 95/14703

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/311

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO,A,84 04996 (SOBCZAK) 20 December 1984 see page 8, line 12 - page 9, line 1 ---	1-4
X	JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY: PART B, vol. 10, no. 6, December 1992 NEW YORK US, pages 2393-2397, XP 000331694 WONG ET AL 'Fabrication of sub-20 nm trenches in silicon nitride using CHF3/O2 reactive ion etching and oblique metallization' see sections IV. and V. on pages 2394 to 2396 --- -/--	1,2,4

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
7 March 1996	21.03.96
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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 95/14703

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,4 966 870 (BARBER ET AL) 30 October 1990 cited in the application	1,2,4,5
X	& EP,A,0 337 109 (BARBER ET AL) 18 October 1989 see page 4, line 14 - line 31 ---	1,2,4,5
A	JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY: PART A, vol. 9, no. 3, June 1991 NEW YORK US, pages 775-778, XP 000359402 DULAK ET AL 'Etch mechanism in the reactive ion etching of silicon nitride' see figures 3,4 ---	1-12
A	IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, vol. 6, no. 3, August 1993 NEW YORK US, pages 290-292, XP 000399832 RILEY ET AL 'Reactor characterization for a process to etch Si3N4 formed on thin SiO2' see figure 7 ---	1-12
A	US,A,4 897 365 (BALDI ET AL) 30 January 1990 cited in the application	3,10
A	& GB,A,2 165 992 (BALDI ET AL) 23 April 1986 see abstract ---	3,10
A	US,A,4 484 979 (STOCKER) 27 November 1984 see abstract ---	1-12
A	PATENT ABSTRACTS OF JAPAN vol. 17 no. 140 (E-1336) ,22 March 1993 & JP,A,04 309221 (TSUKAMOTO) 30 October 1992, see abstract -----	1-12

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 95/14703

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